

IEEE 802.15.4/ZigBee™ Compliant IF Limiter and Received Signal Strength Indicator for RF Transceivers

Rajshekhar Vaijinath, Ashudeb Dutta and T K Bhattacharyya

Advanced VLSI Design Laboratory

Indian Institute of Technology Kharagpur-721302 (India)

Email:rajshekhav@yahoo.com

Abstract—This paper presents a low-voltage, low-power CMOS circuit for an intermediate frequency (IF) limiting amplifier and received signal strength indicator (RSSI). Using a single 1.8-V supply voltage, simulated results demonstrate the input dynamic range is larger than 80 dB and a sensitivity of around -80dBm. A low intermediate frequency of 2 MHz is chosen for our application. Power dissipation is 6mW and the input referred noise is 16 μ V. The prototype is implemented using a 0.18 μ CMOS technology. This architecture is designed for RF transceivers complying IEEE 802.15.4/ ZigBee™

Keywords:-Detector, IF Amplifier, RSSI, Wireless Communication

I. INTRODUCTION

ZigBee™ is a new wireless networking standard which will enable a new set of radio products for low cost and low power. ZigBee™ uses the radio protocol defined by IEEE 802.15.4 [1].

Wireless communication has grown in terms of both user volume and technology. Advanced technologies have offered reduced weight, smaller size, and increased battery life. We require an architecture with greater received signal strength accuracy, increased signal dynamic range, improved temperature stability for measuring received signal strength and for detecting frequency interference which is operable at lower supply voltage. Because the supply voltage for transceivers is becoming lower and lower in near future [2].

The architecture of the limiting amplifier and RSSI employed here is determined by the optimal power consumption for a specified speed, overall gain and accuracy. Each gain cell of the limiting amplifier employs folded diode load for low-voltage operation. Full-wave current rectification and summation are employed in the RSSI circuit to achieve high precision while maintaining low voltage and low power.

The RSSI is generally realized in logarithmic form because the wide dynamic variation of the received signal can be represented within a limited

indication range. Successive-detection architecture is adopted for realizing the logarithmic amplifier. It is essentially composed of several full-wave rectifiers and a low-pass filter, which are in combination with the existing limiting amplifier circuits. Thus successive-detection is power efficient [3].

The traditional implementations of logarithmic amplifiers are temperature dependent. Therefore we use the successive-detection architecture [4], wherein the sum of equally weighted taps along a cascade of identical clipping amplifiers approximates the logarithm as a piecewise-linear function. A DC measure of the amplitude of a bipolar signal such as a sine wave is obtained by rectifying each tap, and low pass filtering the sum of the rectified taps. These measurements will be accurate to the degree the actual amplifier input-output characteristic conforms to the ideal logarithm [5] and how stable it remains over the operating temperature range.

RSSI is used to adjust automatically the gain of the RF front-end (LNA) on its own or this information is sent to the base station to regulate the transmitted power level and to determine cell handoff.

In this paper the design method for a intermediate frequency amplifier and full wave rectifier, consisting of two identical unbalanced source coupled pairs with the cross coupled input stage and parallel connected output stage in CMOS technology, which can operate at lower supply voltage, 1.8V is discussed. The results of intermediate frequency amplifier and logarithmic amplifier are used for practical purposes [6].

Our design is more suitable for sensor network applications. Sensor network is also a part of Ad-Hoc network which is self organized and self handling for low data rate applications such as home automation, interactive devices, personnel health care, consumer electronics, automated fire containment, industrial monitor and control [7].

II. ARCHITECTURE DESIGN

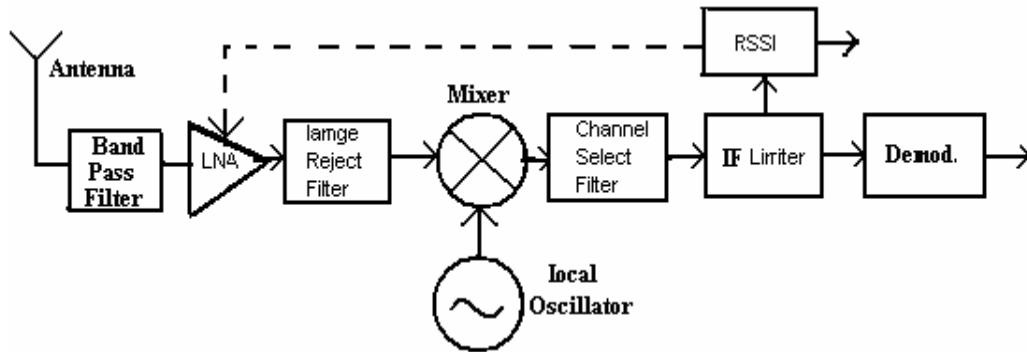


Fig1 A typical receiver architecture

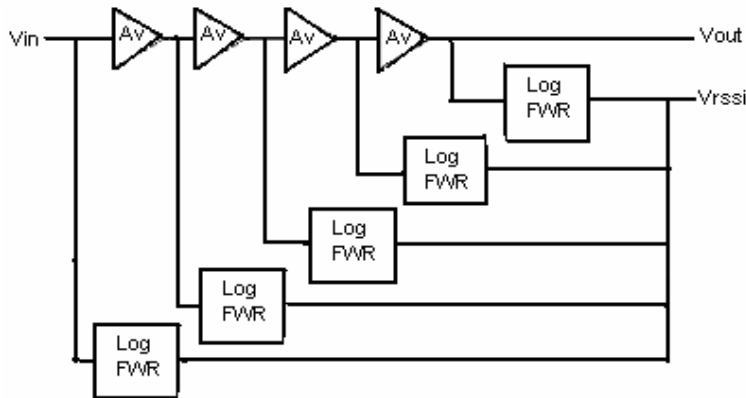


Fig2. RSSI with IF limiter block diagram (Successive detection architecture)

Fig1 shows, the architecture of a typical modern receiver system. The IF limiting amplifier/received signal strengths indicator system is shown in the fig2. The circuit works because of the limiting nature of the amplifier, and the logarithmic response of the RSSI stages. The amplifier takes the input signal and amplifies it so that the amplitude variations disappear and the phase variations of the signal of interest are all that are left. Most of the receiver gain and bandwidth is achieved by IF limiting stage. The gain of the last stage starts falling off for any more increase in the input signal, and so the input to the last stage does not change much when it passes through the last stage. When the second stage starts limiting, the same thing happens until the circuit has no gain because it is in saturation.

The RSSI stages rectify the signals from each stage and change the signal to a current. The output of each stage of the RSSI is fed to a resistor to ground, which performs a summing operation. The RSSI stages output less current for an increase in input voltage, so when the amplifier stages go into limiting, the RSSI stages are at their minimum current level. Thus a logarithmic indication of

signal strength is output. The last stage will start going into limiting first because it will have the product of the gains of the first two stages to boost the signal high enough.

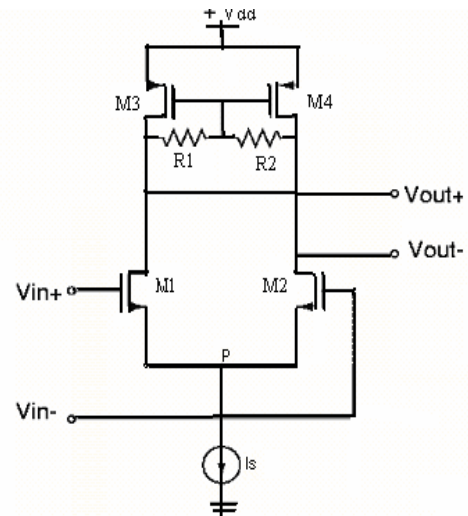


Fig3 IF Amplifier

Low IF frequency is chosen compared to radio frequency. Because the advantage is, radio frequency

is not directly down converted to base-band, DC offset problem and flicker noise critically does not affect the receiver performance. Further, since IF is very low compared to radio frequency the image is very far from the IF band and hence very low Q requirements of the filters which can be implemented off-chip.

III. CIRCUIT DESIGNS

A. Intermediate Frequency Limiting Amplifier

A gain stage of the limiting amplifier can be a conventional simple source-coupled pair shown in fig3. This structure alleviates the dynamic range requirement of the analog-to-digital interface.

A limiting amplifier composed of a chain of gain stages saturates the input signal to a constant level. Power minimization in the IF stage of wireless application is more a practical issue. Once the stage number increases, the total power increases linearly. The intermediate frequency amplifier has four stages, so that a high gain is not required for a single stage and RSSI simulations can be made accurately. The gain of IF amplifier depends upon the aspect ratios of transistors M1 and M2 which can be explained by the equation

$$A_v = \sqrt{\frac{W1/L1}{W2/L2}} \dots (1)$$

Theoretical gain plot of IF limiter is shown in fig4

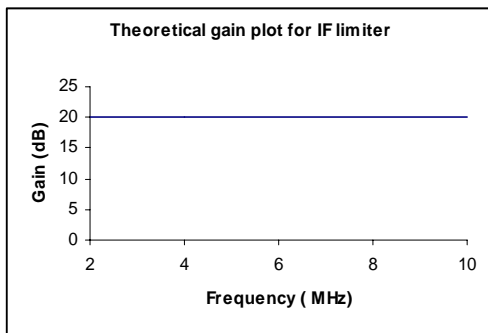


Fig4 Theoretical gain plot for IF limiter

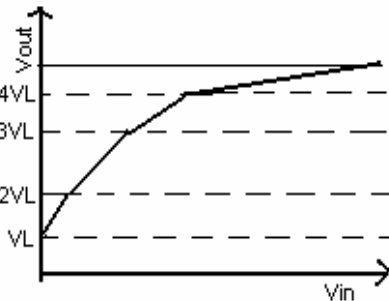


Fig5. Piecewise linear approximation to log function. VL is the clipping level of each amplifier

B. Received Signal Strength Indicator

Fig5 is a piecewise linear approximation to logarithmic function. Each piece of linear section is obtained by rectifying each gain cell output of the limiting amplifier first. All the rectified waveforms are then summed and filtered to yield a dc-like indicating voltage. The RSSI schematic shown in fig6 is basically a logarithmic full wave rectifier. The circuit is made up of an un-balanced source coupled pairs with cross-coupled outputs, whose inputs are connected in parallel.

With no input present, the current output from the circuit is at its maximum value. The output current decreases as the input voltage increases. Since the source-coupled pairs are unbalanced, the wider MOSFETs consume most of the bias current. Since the drains of the larger NMOSFETs are tied together, the current flowing in the right hand mirror is larger than the current in the left hand mirror. As the input voltage is increased, the narrower MOSFETs have a greater relative increase in current than the wider MOSFETs, and so there is a decrease in the amount of current flowing in the output of the right hand current mirror. Thus resembles to logarithmic nature.

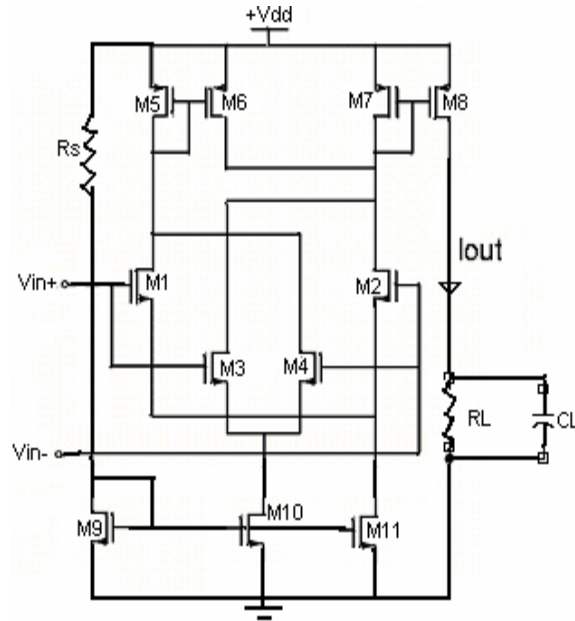


Fig 6. Logarithmic full wave rectifier

It is assumed that all transistors are operating in saturation region. Different output currents for $|\Delta I| \leq I_o$ is obtained. Where 'Io' is the current source used for biasing. The restricting parameter $k > 1$ is used for scaling the transistors. The notations x and y are used for currents in order to have simple mathematical simplifications. $\beta =$ Transconductance parameter & is modeled as

$$\beta = \beta_0 \left(\frac{T}{T_0} \right)^{\frac{3}{2}} \text{ where } T=300^0\text{K,}$$

$\beta_0 = \beta$ at temperature T_0

I_{D1} and I_{D2} are the drain currents of M1 & M2 transistors

k =Scaling factor and

$$x = I_{D1}, y = I_{D2}$$

$$\sqrt{x} - \sqrt{ky} = V_1 \sqrt{\beta} k = a, \quad x + y = I_0 = b$$

Where 'a' and 'b' are constants taken for mathematical simplification and the difference current is $x-y = \Delta I_1$.

The differential input voltage is given by the relation $V_{GS1} - V_{GS2} = V_{in1} - V_{in2} = V_1$

$$V_{GS1} = \sqrt{2I_{D1}/\beta} + V_{tn}, \quad V_{GS2} = \sqrt{2I_{D2}/\beta} + V_{tn}$$

$$V_1 = \sqrt{I_{D1}/k\beta} - \sqrt{I_{D2}/\beta} \quad \dots\dots\dots(2)$$

Solving for 'y' using quadratic relation

$$y = \frac{a^2 k + (k+1)b - a^2 \pm 2a\sqrt{k(k+1)b - ka^2}}{(k+1)^2}$$

In the first case when the input differential voltage is increased the current available at the second current mirror is the difference between I_{D1} and I_{D2} and designated as ΔI_1 , therefore $\Delta I_1 = I_{D1} - I_{D2}$

$$= \frac{(k-1)(k+1)I_0 - 2k\beta V_1^2 \pm 4k\beta V_1 \sqrt{(K+1)\frac{I_0}{\beta} - KV_1^2}}{(K+1)^2} \left(-\sqrt{\frac{I_0}{\beta}} \leq V_1 \leq \sqrt{\frac{I_0}{K\beta}} \right)$$

$$\Delta I_1 = I_0 \operatorname{sgn}(V_1) \left(|V_1| \leq -\sqrt{\frac{I_0}{\beta}}, \sqrt{\frac{I_0}{K\beta}} \leq V_1 \right) \dots\dots(3)$$

For different values of $K=4, 9$ and 16 the DC transfer curves in hand calculation is as shown in fig7.

The precision of the RSSI is mainly determined by the number of stages of the limiting amplifier. The maximum error compared with an ideal logarithmic curve can be derived as

$$\text{Error}_{\max} (\text{dB}) =$$

$$10 \left[(-1 + \sqrt{A_3 + A_3}) \log A_3 - (A_3 - 1) \log A_3^{(3A_3 - 1)/(2A_3 - 2)} \right] / A_3 - 1$$

where A_3 is the gain of each stage as shown in fig8. Using four stages in the architecture, the voltage gain 80 dB of can be determined. The relative error in RSSI is around ± 1 dB, which is satisfactory for our sensor application.

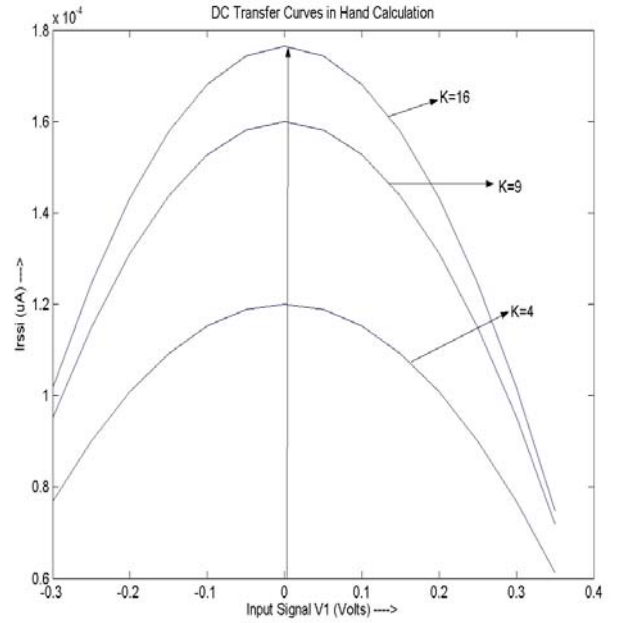


Fig 7: DC transfer curves in hand calculation with parameters $K=4, 9$ and 16

IV. EXPERIMENTAL RESULTS

The limiting amplifier and RSSI are implemented in a standard 0.18u CMOS technology. Fig9 shows the simulated output characteristics of IF Limiter. Each stage of IF limiter provides a voltage gain of 20 dB. Input referred noise is $16\mu\text{V}$ as shown in fig10. A high sensitivity of around -81dBm is achieved. The power consumption is 6mW using a 1.8V single supply voltage. An external resistor of 500Ω and a 25 pF capacitor are used to convert the summed RSSI current to voltage and simultaneously extract the dc current as shown in fig11. The indication range is wider than 80 dB shown in fig12. Table-I lists the performance parameters of IF amplifier and RSSI.

Table-I

Performance parameters of IF Amplifier/RSSI

Technology	0.18u CMOS
IF amplifier	
Single stage gain	20dB
Single stage bandwidth	10MHz
Input referred noise	$16\mu\text{V}_{\text{rms}}$
-3dB sensitivity	-81dBm
RSSI	
RSSI dynamic range	> 80dB
Logarithmic linearity error	± 1 dB
Supply voltage	1.8V
Power dissipation	6mW

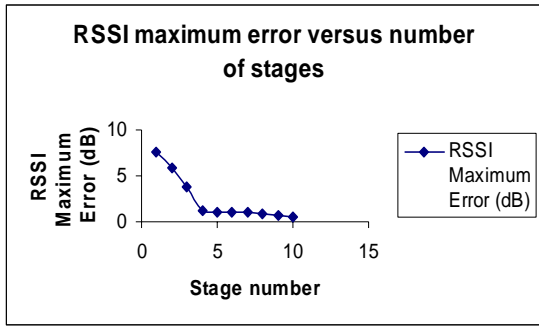


Fig8. RSSI maximum error versus number of stages

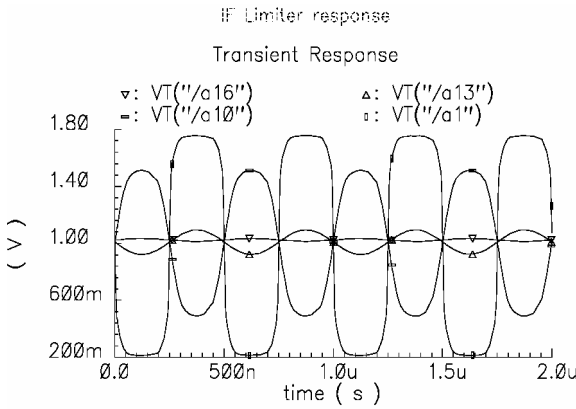
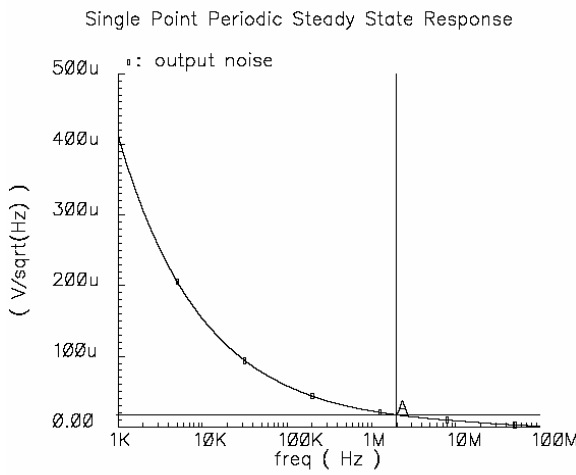


Fig9. Simulated output characteristics IF Limiter



A: (1.99936M 16.8044u)

Fig10 Simulated input referred noise

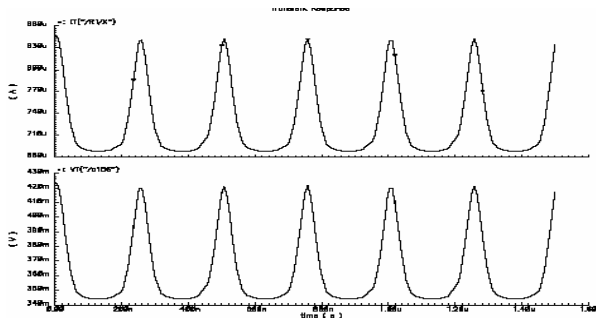


Fig11. Rectified output of the full wave rectifier

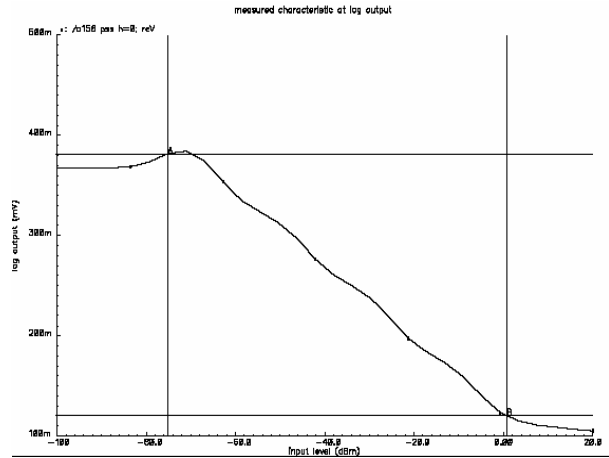


Fig12. Simulated RSSI Transfer curve and linearity

From the fig12 it is clear that the dynamic range of the successive detection structure is limited on the upper end when the input causes the first stage in cascade to clip and on the lower end when all stages are in linear region.

V. CONCLUSION

Low voltage, low power CMOS circuit design for 2-MHz IF amplifier and RSSI applications were presented in this paper. Four stage architecture is derived under minimum power consideration. Each gain cell employs folded diode load structure a for supply voltage of 1.8V. IF limiters with current mode full wave rectifiers constitute the RSSI successive detection architecture. Sensitivity of -81dBm and an indication range of 80 dB within 1-dB linearity error were observed. The input referred noise was found to be 16 μ V. The prototype is implemented in 0.18 μ CMOS technology and consumes a power of 6.0 mW.

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